A 3D Interconnect System for Large Biosensor Array and CMOS Signal-Processing IC Integration

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Abstract

In this paper, two new interconnect technologies designed for integration of a large biosensor array and a signal processing CMOS IC are presented; a TSV technology that can be fabricated in wafers that cannot be aggressively thinned down or have sensitive sensors fabricated in prior processes, and a compliant interconnect technology that enables minimal stress permanent interconnections or low-force temporary interconnections to allow reuse of CMOS ICs. In addition, integration of TSV to a silicon nanowire label-free biosensor is demonstrated.

I. Introduction

3D integration has been a critical area of research within the semiconductor community during the last decade. With the promise of increased performance, increased functionality and new innovative systems that were not possible before, it is an extremely appealing concept. While much of the focus and progress have been in the area of vertically integrating two or more CMOS ICs, its benefits are drawing interest to another area of 3D integration – heterogeneous integration of a sensor array and a signal processing CMOS IC.

There is a strong interest in such integration because in many fields, having a large array of sensors or MEMS not only improves the performance of existing systems but it also allows completely new type of systems to be created, capable of making new type of measurements. However, due to the limited I/O density and poor performance of 2D interconnect systems that connect an array of sensors to a signal processing CMOS IC, much of this effort has not yet been realized.

Monolithically integrating sensors on top of a CMOS IC has allowed some progress but the integration of an arbitrary sensor process to a CMOS process can be complex and severely limits the materials and processes accessible to the sensor designers and often, the integration is done with a legacy CMOS process [1]. Heterogeneous integration on the other hand allows the sensor array and CMOS to be fabricated independently, eliminating such limitations and yet, it still offers similar benefits. However, in order to integrate sensor array with a CMOS IC, a new interconnect system is needed that can fulfill requirements outlined below.

II. Interconnect Requirements

To begin with, sensors often require exposure to the environment for sensing and as a result, a back-to-front integration scheme is the most desired method of integration, which requires a TSV technology. However, many of the current TSV technologies exploit the fact that wafers are aggressively thinned down and unfortunately, many of the sensors or MEMS require thick wafers in order to avoid severe chip warpage or, simply because it has deep trench structures that are several hundreds of microns deep. As a result, for integration with an arbitrary sensor, the TSV process will need to be able to deal with relatively thick wafers.

There is also the issue of when these TSVs should be fabricated; the TSV-First approach, where the TSVs are fabricated prior to the sensor, is difficult as some sensors involve a process, such as a high temperature process, that may not be compatible with the TSV process especially if Cu is to be used as the conductor. At the same time, TSV-Last approach is also difficult, as the Chemical Mechanical Planarization (CMP) process, a critical process in many TSV technologies, can damage the sensitive sensor structures. Developing a TSV technology that can eliminate the need for CMP, even if it is on the sensor side only, can be beneficial when it comes to integration using the TSV-Last approach.

Currently available interface interconnect technologies between the CMOS IC and the sensors/MEMS are also inadequate as they have been known to induce thermomechanical stress causing die warpage and for sensors such as piezoelectric sensors, these warpage can cause unwanted noise in the signal. Therefore, an interface interconnect technology capable of isolating the sensors/MEMS from the thermomechanical stress is highly desirable [2].

There is also an interest in a temporary interface interconnection so that the CMOS IC can be reused while the contaminated biosensor chips are replaced in order to reduce the unit cost of testing. This means that the interface interconnects should have some compliance to allow low-force and low-resistance electrical connections without getting damaged during the repeated assembly process.

In this paper, we present two new interconnect technologies that are part of our proposed sensor/CMOS

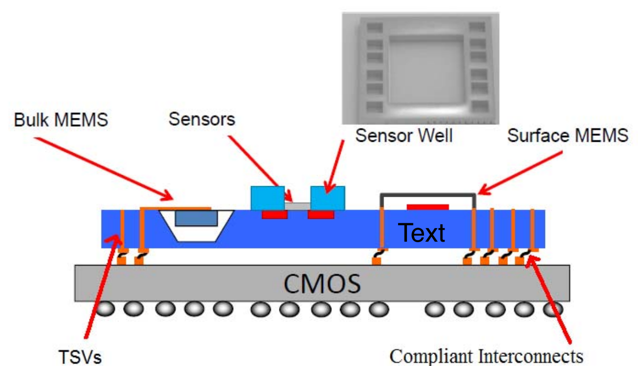

Figure 1. Proposed 3D integration scheme for sensor, MEMS and CMOS IC integration showing its interconnect system; TSVs and compliant interconnects.

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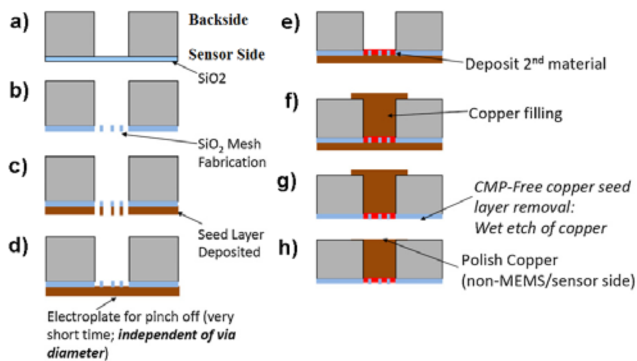

Figure 2. Process flow for TSV technology under consideration

integration scheme (Figure 1); a novel TSV technology and a mechanically flexible (compliant) interconnect technology. With the focus being the integration with biosensors, we describe and integrate the TSV technology with a silicon nanowire label-free biosensor that can benefit enormously from 3D integration with a CMOS IC. We also present a novel compliant interconnects that can be used to make temporary electrical connections allowing contaminated sensor array to be discarded while reusing the CMOS circuitry.

III. TSV for Sensor/MEMS and CMOS IC Integration

a) Process Description

In the TSV technology under consideration, we address two common issues that arise when integrating with a sensor on a wafer that has not been aggressively thinned down like CMOS wafers; deposition of an electroplating seed layer at the bottom of deep via holes and CMP free planarization on the side of wafer where sensors are present. The proposed process diagram is shown in Figure 2.

The process begins by depositing with PECVD, a 1um layer of SiO_2 on the sensor side of the wafer. Then, a DRIE is used to etch the silicon to form via holes using SiO_2 layer as the etch stop layer. The SiO_2 layer is now suspended over the etched via hole (Figure 2a). After the via hole formation, a mesh pattern is etched on the suspended SiO_2 layer using RIE, as shown in Figure 2b and 3a. At this point, the sidewall of via holes can be passivated using either a thermal oxidation process or a PECVD process if the existing sensors are sensitive to high temperature processes. In order to form an electroplating seed layer from this mesh patterned SiO_2 layer, a 300A/2000A layer of Ti/Cu is deposited on the sensor side using an e-beam evaporator. E-beam evaporator was used in order to avoid deposition on the sidewall of via holes. Then, with a non-conductive tape covering the back side, copper is electroplated until the mesh is "pinched off" as shown in Figure 2d and 3b. After the "pinch off", the non-conductive tape is now placed on the sensor side and a layer of Ni is electroplated from the bottom of the vias. This layer will be used later as a wet etch stop layer to remove the copper seed layer. Once the nickel layer is formed, Cu is then electroplated until via holes are completely filled. The wafer is then dipped in Al Etchant Type A solution until all the seed layer is removed and electroplated Ni layer is revealed. The sample is then dipped in BOE to remove the SiO_2 mesh layer. Finally, CMP is performed on the back side to remove the excess Cu from electroplating.

So far this process has been successfully fabricated without voids and electrically tested in a 400um thick wafer with 50um diameter vias, with ongoing research to reduce the pitch to 10um thereby enabling up to 10^6 TSVs per 1cm x 1cm chip.

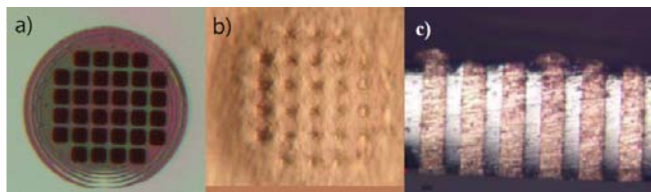

Figure 3. a) Mesh patterned on the suspended SiO_2 layer. b) "Pinched off" Cu seed layer. c) TSV cross-section showing void-free via filling.

b) Process Integration with a Silicon Nanowire Biosensor

Silicon Nanowire (SiNW) sensor is a label-free biochemical sensors that can benefit from 3D integration. Like other label-free sensors, SiNWs operate by detecting a property inherent to a biomolecule. More specifically, they detect the electrical charge associated with proteins, nucleic acids, and other biomolecules that are in a pH different than their isoelectric point. The advantage of label-free sensors in general is in their ability to work without the constraints of conventional labels like flurophores. Label-free sensing enables the simultaneous detection of an essentially unlimited number of target molecules on one chip with remarkable sensitivity extending into the sub 100 femtomolar range [3]. The more specific advantage of SiNW sensors compared to other label-free sensors such as those that are mass-based or optical-based is on their easy integration with conventional solid-state, top-down, Si CMOS processing.

One of the key advantages to a top-down fabricated label-free sensor is how naturally it lends itself to arraying numerous sensors on a single chip. Such arrays would effectively enable the biological assays conducted on current platforms like microwell plates to be performed on a substantially smaller chip. This has numerous advantages including smaller required volumes of analytes and the capability to detect sustainably more target molecules such as cancer markers or single nucleotide polymorphisms on a single chip. As we enter the era of personalized medicine, these are promising advantages. However, there is a need for a packaging method that enables both a very high density array of sensors and a means to separate the aqueous environment of the sensing side from the controlling circuitry. The TSV technology described in the previous section and our integration scheme (Figure 1) represents such method.

There are several challenges and constraints when integrating a TSV process with the SiNW biosensor; first, the sensor fabrication process involves a high temperature (900°C) process, meaning that if Cu was to be used as the

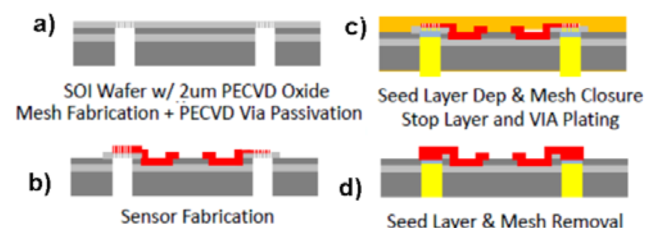

Figure 4. Process Flow for integrating SiNW with TSV.

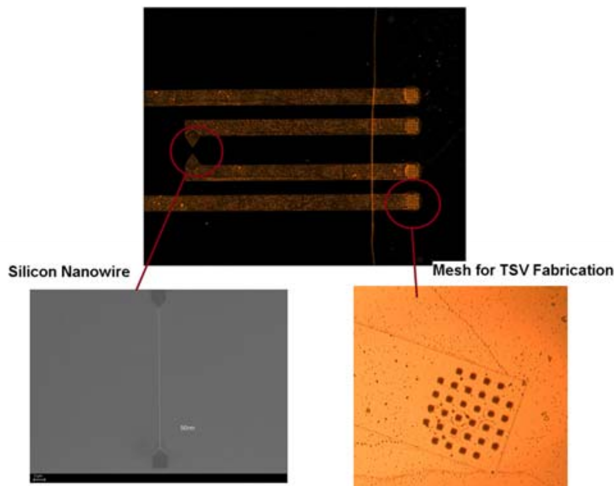

Figure 5. Images of SiNW and TSV mesh based TSV is integrated

TSV conductor, electroplating to fill the via will need to be done after the sensors. Having vias filled last means that a CMP process is not viable on the same side of the wafer, which is possible with the TSV technology presented in this paper.

With above constraints in mind along with an access only to a FEOL safe DRIE tool, a process flow was developed as shown in Figure 4. Figure 5 is an optical image of a fabricated SiNW sensor adjacent to the mesh pattern for the TSVs, which enables back side interconnection for the sensors and where we envision a CMOS IC will perform all signal processing, conditioning, and execution.

IV. Compliant Interconnects for Sensor/MEMS to CMOS IC Interconnection

Compliant interconnects play an important role in the overall 3D integration scheme described previously (Figure 1). For applications where temporary connection is desired, its compliance can be engineered to provide the low force, low resistance electrical connection. For applications where permanent interconnection is desired, its compliance can minimize the thermomechanical stress without the use of an underfill. For cases, its compliance and large standoff height (up to 20um) allows interconnection to a wafer surface that may not be highly uniform [4].

Fabrication of compliant interconnects start with forming of sacrificial polymer domes formed by spin coating and patterning a photodefinable polymer on a Si wafer. After reflowing the polymer, a metal seed layer is deposited and a layer of thick resist is spin coated and patterned with the shape of the compliant interconnects on top of the polymer domes. Depending on the desired compliance, 7 to 25um of Cu or Au is then electroplated.

With this technology, it is also possible to form solder balls on top of compliant interconnects. For this, SU-8 is spin coated and patterned on top of the electroplated interconnects to form polymer dams which act as a solder mask to confine the solder ball to the solder pad area only. A thick resist is spin coated and patterned to expose the opening inside the polymer dam, and Ni and eutectic solder are electroplated. After removing the seed layer and the sacrificial polymer, and the solder is then reflowed.

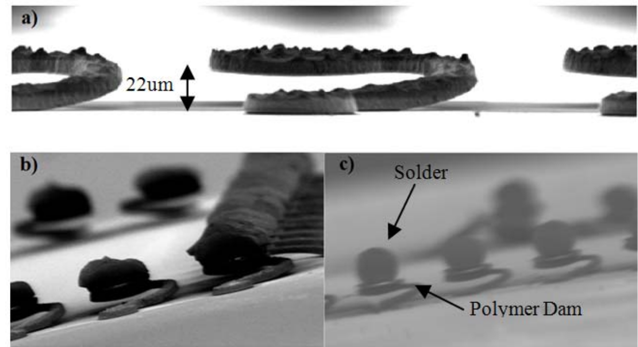

Figure 6. a) Compliant interconnects showing ~22um stand off height. b) interconnects with solder ball before reflow. c) interconnects with solder ball after reflow

ANSYS FEM results shows that compliance of a 8um thick interconnect is ~15mm/N. Multiple compliance measurements on one test die using a nanoindentation tool showed an average compliance of 16.7mm/N with a standard deviation of 0.42 and has not shown signs of yielding when it is displaced by 3.5um vertically (limit of the measurement tool). So far, the compliant interconnect with pitch of 100um x 50um and standoff height of 22um has been successfully fabricated.

V. Conclusions

In this paper, an interconnect system comprised of a TSV technology and compliant interconnect technology, is presented that enables the “marriage” of sensor/MEMS and CMOS – a step into the era of “more than Moore.”

A TSV technology is presented that can form a seed layer in deep via holes and a CMP-free planarization technique that allows vias to be fabricated after the sensor allowing maximum material and process freedom for the sensor designers. The benefits of these two techniques are experimentally demonstrated by integrating it with a SiNW label-free biosensor.

A compliant interconnect technology is also presented that allows low-force and low resistance temporary electrical contact so that the CMOS IC can be reused while the contaminated sensors are discarded. The same interconnect system can be used to make a stress-isolating permanent electrical connections.

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